wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein said first circuits are fed said internal supply voltage, wherein the magnitude of said internal supply voltage changing at said second rate is [not smaller but] larger than that of said internal supply voltage changing at said first rate, wherein said internal supply voltage changing at said third rate enables testing of said first circuits, and wherein the magnitude of said internal supply voltage up to said third rate becomes larger without decreasing [in proportion to an enlargement of said] as the magnitude of said external supply voltage increases.

Claim 12, line 9, delete ";" and insert -- , --;
line 26, delete ";" and insert -- , --;
line 29, delete ";" and insert -- , --;
line 35, delete ";" and insert -- , --;
line 41, delete ";" and insert -- , --.

13. (three times amended) A semiconductor integrated circuit comprising:

a chip;

load circuits provided on said chip;

internal power supply means provided on said chip for reducing an external supply voltage to an internal supply voltage smaller than said external supply voltage within said chip and supplying it to said load circuits[;],

wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is [not smaller but] larger than that of said internal supply voltage changing at said first rate, wherein said internal supply voltage changing at said third rate enables testing of said load circuits, and wherein the magnitude of said internal supply voltage up to said third rate becomes larger without decreasing [in proportion to an enlargement of said] as the magnitude of said external supply voltage increases.

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~~19.~~ (twice amended) A semiconductor integrated circuit comprising:

a chip

load circuits [provide don] <u>provided on</u> said chip;

internal power supply means provided on said chip for reducing an external supply voltage to an internal supply voltage smaller than said external supply voltage within said chip and supplying it to said load circuits[;]⊥

wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at [as] <u>a</u> first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is larger than that of said internal supply voltage changing at said first rate and wherein said internal supply voltage changing at said third rate enables testing of said load circuits[;]⊥

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wherein the change of said internal supply voltage is made inside of said internal power supply means by detecting a change in said external supply voltage[;]⊥

wherein, when said external supply voltage is between said level exceeding said first voltage and said second voltage, said load circuits are in normal operative states, and wherein, when said external supply voltage exceeds said second voltage said load circuits are in aging tests[;]⊥

wherein the third rate of change of said internal supply voltage when said external supply voltage is between a level exceeding said second voltage and a predetermined third voltage is higher than a fourth rate of change of said internal supply voltage after said external supply voltage exceeds said third voltage[;]⊥

wherein, when said external supply voltage is between said first voltage and said second voltage, said internal supply voltage is substantially constant.

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~~20.~~ (three times amended) A semiconductor integrated circuit comprising:

a chip;

a first circuit provided on said chip;

a second circuit provided on said chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is smaller than an external supply voltage;

a reference voltage generating means, provided on said chip, for generating a reference voltage[;]⊥

wherein said reference voltage provided by said reference voltage generating means is fed to said internal

power supply means, said internal supply voltage provided by said internal power supply means is fed to said second circuit, and said external supply voltage is fed to said first circuit, wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is [not smaller but] larger than that of said internal supply voltage changing at said first rate, wherein said internal supply voltage changing at said third rate enables testing of said second circuit, and wherein the magnitude of said internal supply voltage becomes <u>up to said third rate</u> larger without decreasing [in proportion to an enlargement of said] <u>as the</u> magnitude of said external supply voltage <u>increases</u>.

24
~~21~~. (three times amended) A semiconductor integrated circuit comprising:

a chip;

a first circuit provided on said chip;

a second circuit provided on said chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is smaller than an external supply voltage;

a reference voltage generating means, provided on said chip, for generating a reference voltage[;]_

wherein said reference voltage provided by said reference voltage generating means is fed to said internal power supply means, said internal supply voltage provided by said internal power supply means is fed to said second circuit, and said external supply voltage is fed to said first circuit, and a breakdown voltage of a first transistor having <u>fed</u> thereto said external supply voltage is higher than a breakdown voltage of a second transistor having fed thereto said internal supply voltage, wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is [not smaller but] larger than that of said internal supply voltage changing at said first rate, wherein said internal supply voltage changing at said third rate enables testing of

said second circuit, and wherein the magnitude of said internal supply voltage up to said third rate becomes larger without decreasing [in proportion to an enlargement of said] as the magnitude of said external supply voltage increases.

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~~32~~. (three times amended) A semiconductor integrated circuit comprising:

a substrate;

a first circuit, provided on said substrate, having a first transistor; a second circuit, provided on said substrate, having a second transistor;

an internal power supply means, provided on said substrate, for supplying an internal supply voltage which is smaller than an external supply voltage;

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a reference voltage generating means, provided on said substrate, for generating a reference voltage;

wherein said internal supply voltage provided by said internal power supply means is fed to said second circuit, said external supply voltage is fed to said first circuit and said internal power supply means includes a converter transistor which outputs said internal supply voltage, said converter transistor having a control electrode; and

wherein said internal supply voltage is controlled by said reference voltage supplied to said control electrode of said converter transistor, wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of

said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is [not smaller but] larger than that of said internal supply voltage changing at said first rate, wherein said internal supply voltage changing at said third rate enables testing of said second circuit, and wherein the magnitude of said internal supply voltage up to said third rate becomes larger without decreasing [in proportion to an enlargement of said] as the magnitude of said external supply voltage increases.

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23. (Twice Amended) A semiconductor integrated circuit comprising:

a chip;

an external supply voltage terminal, provided on said chip, for receiving an external supply voltage;

an interface circuit provided on said chip;

an internal circuit provided on said chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is smaller than said external supply voltage;

a reference voltage generating means, provided on said chip, for generating a reference voltage;

wherein said reference voltage provided by said reference voltage generating means is fed to said internal power supply means, wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is [not smaller but] larger than that of said internal supply voltage changing at said first rate, wherein said internal supply voltage changing at said third rate enables testing of said internal circuit and wherein the magnitude of said internal supply voltage <u>up to said third rate</u> becomes larger without decreasing [in proportion to an enlargement of said] <u>as the</u> magnitude of said external supply voltage <u>increases</u>.